International Journal of Microwave and Wireless Technologies

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Compact and ultra-wideband high-efficiency rectifier using asymmetric coupled-line impedance transformer

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Research Paper

Cite this article: Cheng F, Du CH, Wu L, Gu C (2024) Compact and ultra-wideband high-efficiency rectifier using asymmetric coupled-line impedance transformer. *International Journal of Microwave and Wireless Technologies* **16**(6), 966–971. https://doi.org/10.1017/S1759078724000813

Received: 11 July 2023
Revised: 5 August 2024
Accepted: 12 August 2024

Keywords:
power conversion efficiency; rectifier; wideband; wireless power transmission

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Abstract

This paper presents a compact and ultra-wideband high-efficiency microwave rectifier for wireless power transmission (WPT) applications. The input-matching-network utilizes a compact asymmetric coupled transmission line structure, contributing to wideband performance. The rectifier adopts a voltage-doubler topology, resulting in a smooth input impedance across a wide bandwidth. The working principle of the asymmetric coupled transmission line matching network is analyzed. Simulation and measurement are conducted on the proposed rectifier. The fabricated prototype demonstrates a wide bandwidth of 162.5% (0.3–2.9 GHz with the power conversion efficiency (PCE) exceeding 60% at an input power of 18 dBm. Even at an input power of 10 dBm, the measured PCE remains above 50% over the working band. The proposed ultra-wideband rectifier shows promising potential for WPT applications including wireless powering of low-power electronic devices and sensors.

Introduction

Wireless power transmission (WPT) systems have garnered significant attention due to their various applications, including medical sensors, implanted devices, immortal sensor networks, wireless charging electric vehicles, and wireless powering of single-chip systems [1–3]. In the WPT system, the radio frequency-to-direct current (RF-to-DC) rectifier plays an important role as it determines the overall efficiency of the system. Therefore, it is essential to have a rectifier that exhibits both high power conversion efficiency (PCE) and wide operating bandwidth. This ensures coverage for frequency shifts caused by fabrication errors and enables the harvesting of more energy in wireless power harvesting applications.

In order to achieve wideband and high-efficiency performance of a rectifier, the design of the wideband input-matching-network is crucial. Effective impedance matching results in reduced reflected power at the input port. Consequently, a greater proportion of RF power can be converted to DC power, leading to higher efficiency. However, matching a rectifier over a wideband is a challenge because the diode impedance varies with the operating frequency and input power [4]. To address this issue, much research has been carried out recently [5–20]. Most works have focused on the wideband input-matching-network, such as branch-line coupler [5], multistage transmission line [6], series-connected coupled-line [7], nonuniform transmission line [8], L-section matching network [9], series dual-inductive lumped element [10], T-type matching network [11, 17], tapered microstrip line [12], and open/short stub matching network [13]. In papers [8] and [9], lumped elements were adopted in the rectifier design to reduce the circuit size. Minimizing circuit size leads to lower fabrication costs and reduced weight. In contrast to the above methods, Wu et al. proposed a multi-diode structure to realize the wideband rectifier [14]. Each diode can cover a frequency band, and with more diodes, a wider bandwidth may be realized. In paper [19], a broadband and efficient rectifier was realized with minimal interstage matching, which consists of a single short-circuit stub and a virtual battery.

In this paper, a compact multi-octave rectifier with high efficiency is proposed. The asymmetric coupled-line transformer is adopted as the input impedance matching network. It exhibits the merits of compact size and broadband matching. Compared with the design in [17], the proposed rectifier has better reflection coefficient at low frequency. When the rectifier is connected to a receiving antenna with an input impedance of 50 Ω, the rectifier would get more energy when its reflection coefficient is low. For example, if $|S_{11}| = -10$ dB and −15 dB, the signals reflected to the receiving antenna are 10% and 3%, respectively. This implies that approximately 7% more energy can be delivered to the rectifier. For verification, a broadband rectifier is fabricated and measured. The rectifier has dimensions of 19 mm × 18 mm, which is

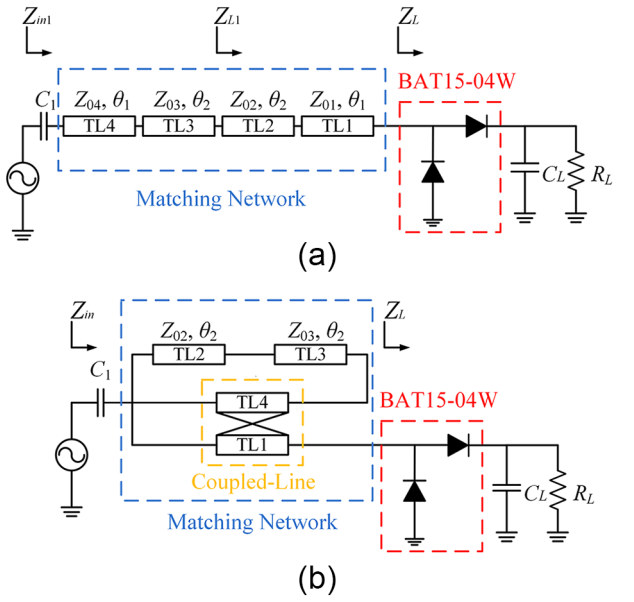

Figure 1. Schematic diagram of the proposed broadband rectifier: (a) without the coupled-line and (b) with the coupled-line.

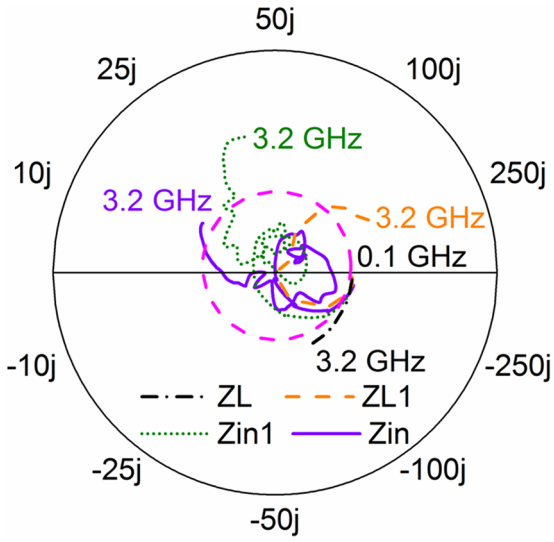

Figure 2. The input and load impedance on the Smith chart.

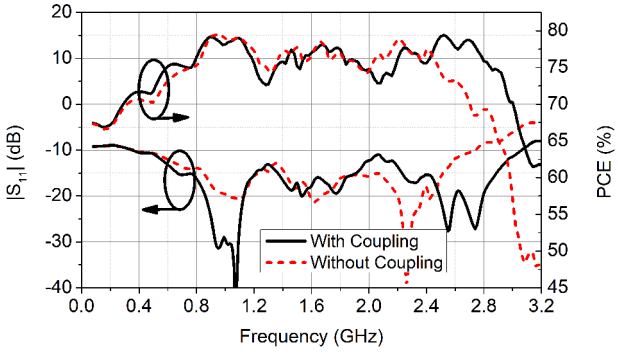

Figure 3. Comparison of $|S_{11}|$ and PCE with and without TL1 and TL4 coupled.

much smaller than those in the previous works. The measured results agree well with the simulated ones. The measured frequency range for $|S_{11}| \leq -10$ dB is from 0.54 to 3 GHz with a relative bandwidth of 139% when the input power is 14 dBm. The measured PCE is exceeding 60% from 0.3 to 2.9 GHz with an input power of 18 dBm. The relative bandwidth for efficiency over 60% is 162.5%. In contrast, the majority of previous works, with the exception [10] and [19], exhibit a relative bandwidth below 100%. Moreover, the measured maximum PCE of the proposed rectifier is 79.8% at 0.9 GHz.

Design and analysis of the wideband rectifier

Compared to the single-diode rectifier topology, the voltage-doubler configuration not only improves the power handling capabilities but also is suitable for achieving broadband performance [8]. Therefore, the Schottky diode BAT15-04W with a series connected pair of diode chips in one package is selected for this design [21]. The design procedure of the proposed broadband rectifier includes two parts, as shown in Fig. 1. In Fig. 1(a), the rectifier is matched by four uncoupled transmission lines labeled TL1-TL4. Each transmission line has a characteristic impedance of Z_{0i} and an electrical length of θ_i ($i = 1$–4). The capacitors C_1 and C_L are used to block the DC and filter the RF signal, respectively. In Fig. 1(b), TL1 and TL4 are coupled. The asymmetric coupled-line impedance transformer not only enhances the compactness of the rectifier but also widens its bandwidth. The rectifier is designed to operate from f_L to f_H with a load of 500 Ω, where f_L and f_H indicate the lowest and highest working frequencies, respectively.

The design strategy of the input impedance matching network is shown in Fig. 2. The start and end frequencies are $f_L = 0.3$ GHz and $f_H = 3$ GHz, respectively. First, the load impedance Z_L is evaluated by the following equation [18]:

$$Z_L = \frac{\pi R_s}{2\theta_{on} - \sin 2\theta_{on} + j\omega R_s C_j (2\pi - 2\theta_{on} + \sin 2\theta_{on})} \quad (1)$$

$$\tan\theta_{on} - \theta_{on} = 2\pi (R_s / R_L) / (1 + 2V_{bi} / V_o) \quad (2)$$

where R_s is the series resistance of the diode, C_j is the diode junction capacitance, and θ_{on} is the turn-on angle of the diode. In Fig. 2, from 0.1 to 3.2 GHz, Z_L is outside the circle where VSWR = 2. Our target is to compress the input impedance trajectory into the circle where VSWR = 2 over a wide frequency range.

To simplify the design process, the coupling between the transmission lines TL1 and TL4 is not considered in the initial stage. The total electrical length of the transmission lines TL1–TL4 is 180° @ 3 GHz, equivalent to 18° @ 0.3 GHz, and its effect at lower frequencies can be neglected. The electrical lengths of the transmission lines θ_1 and θ_2 are set to be 22.5° and 67.5° @ 3 GHz, respectively. To achieve a proper weak coupling, θ_1 is chosen to be shorter than θ_2. In our design, the coupling is approximately −30 dB at low frequencies and −20 dB at high frequencies, respectively. Consequently, it exerts a more pronounced impact on the high-frequency matching of the rectifier. By setting those electrical lengths to be constant, the number of unknown variables can be reduced, and we can solve the characteristic impedance of each transmission line by following procedures.

The transmission lines TL1 and TL2 convert the impedance at the center frequency to be 50 Ω:

$$Z_{L1}((f_H + f_L)/2) = 50 \quad (3)$$

By solving Equation (3), we can get $Z_{01} = 98.48$ Ω, and $Z_{02} = 87.39$ Ω, respectively. After this step, the curve of Z_{L1} from

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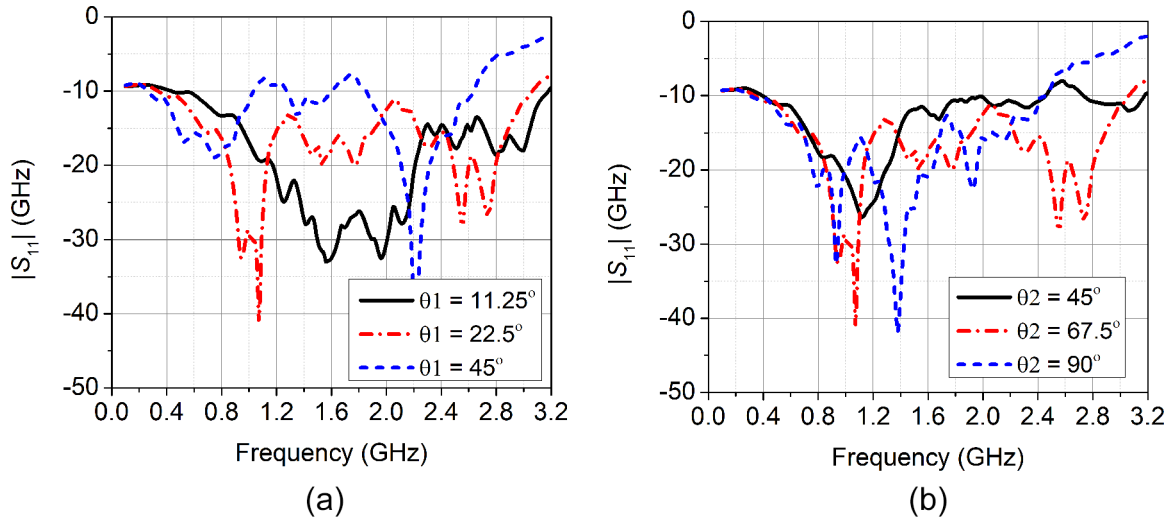

Figure 4. Comparison of $|S_{11}|$ changing with different electrical lengths, (a) θ_1, (b) θ_2.

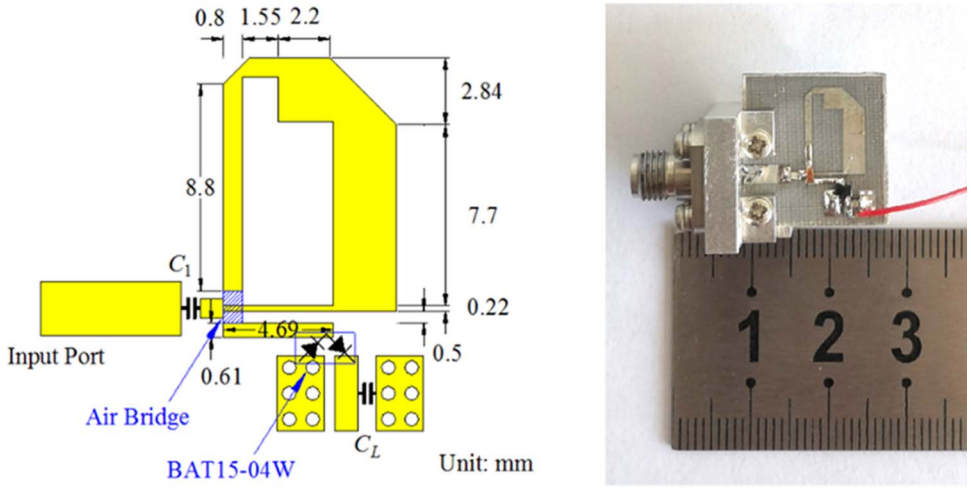

Figure 5. Layout and photograph of the fabricated ultra-wideband rectifier.

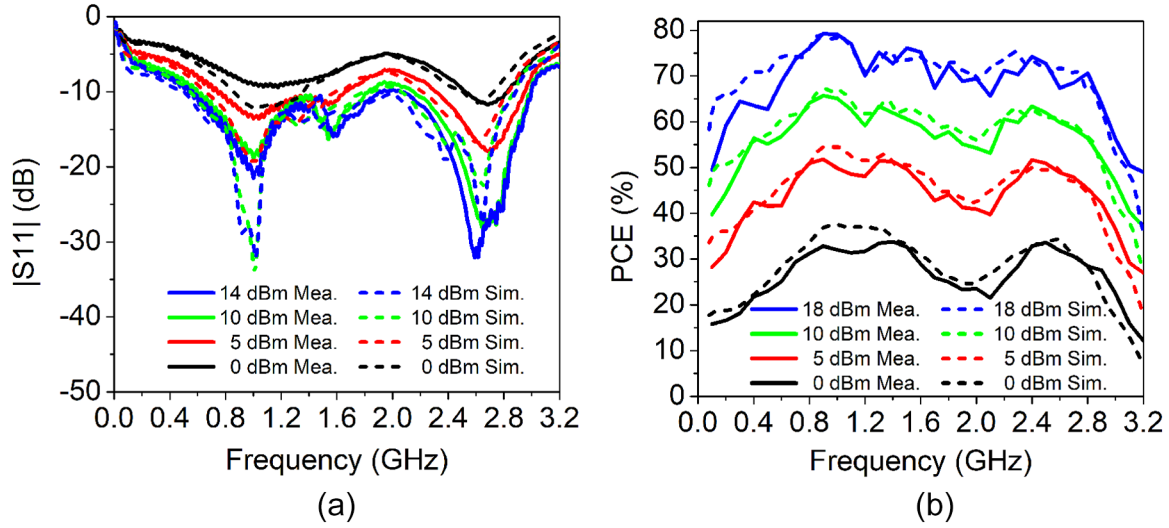

Figure 6. Simulated and measured $|S_{11}|$ and PCE versus frequency at different input power, (a) $|S_{11}|$, (b) PCE.

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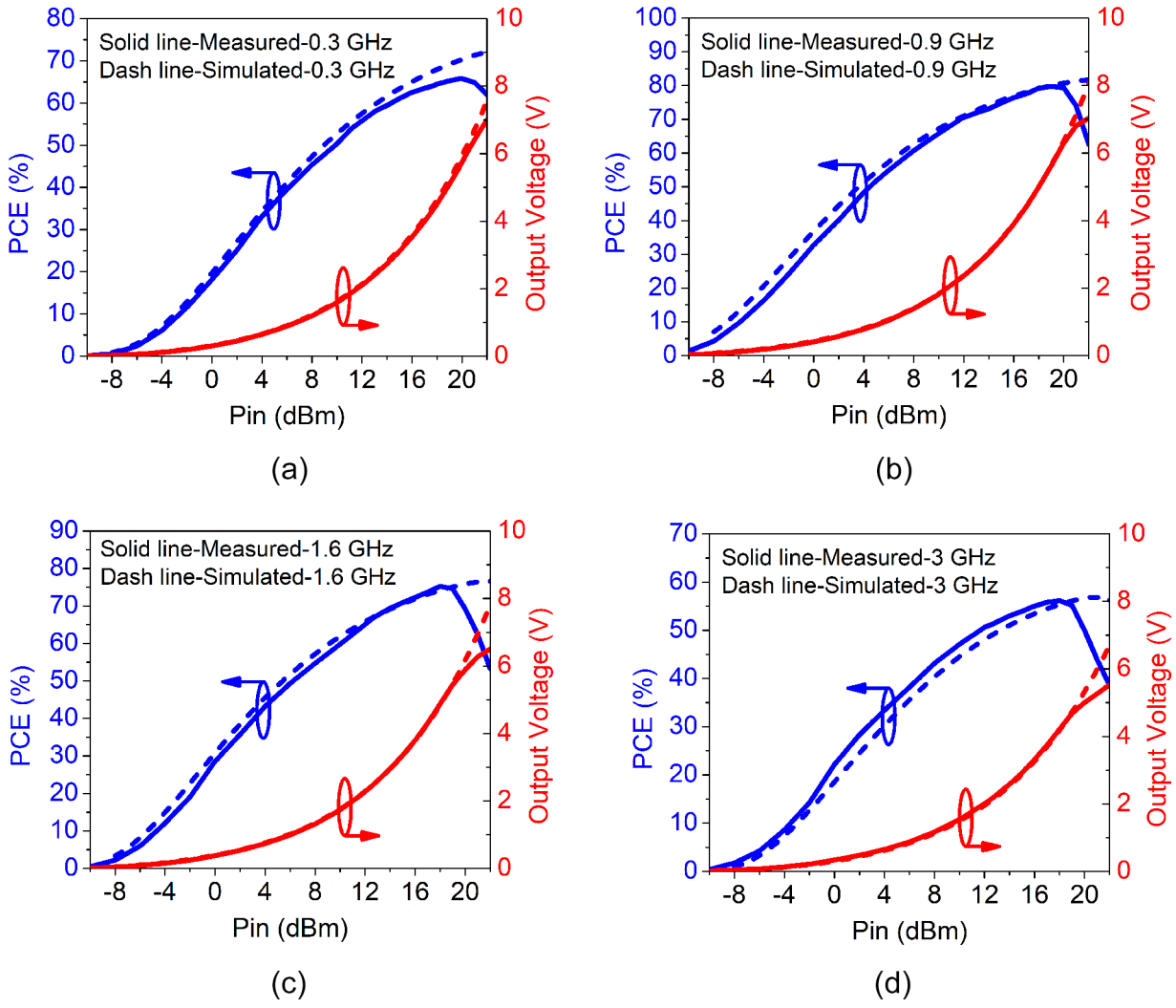

Figure 7. Simulated and measured PCE and output DC voltage versus input power: (a) 0.1 GHz, (b) 0.9 GHz, (c) 1.6 GHz, (d) 3.1 GHz.

0.59 to 2.3 GHz is within the VSWR = 2 circle. Then, the trajectory of Z_{in1} is further compressed to the center of the Smith chart. By solving

$$|\Gamma_{in}(f_L, f_H)| = 2 \tag{4}$$

we can get $Z_{03} = 98.48\ \Omega$, and $Z_{04} = 87.39\ \Omega$, respectively. The bandwidth is broadened to 0.39–2.72 GHz.

Finally, the coupling between TL1 and TL4 is considered to broaden the bandwidth of the rectifier. The coupling has the effect of rotating the trajectory of Z_{in1} anticlockwise on the Smith chart, as shown in Fig. 2. Thus, the impedance at around 3 GHz can be rotated and compressed into the circle where VSWR = 2. When TL1 is close to TL4, the coupling between them is stronger, and weaker when they are farther apart. By using simulation to vary their distance and observing the bandwidth of S11, we can obtain the final design parameters. Figure 3 compares the simulated $|S_{11}|$ and PCE of the rectifier with and without TL1 and TL4 coupled. As shown, with the coupling, the higher frequency edge for $|S_{11}| < -10$ dB can be extended from 2.73 to 3.05 GHz, while the lower frequency edge remains nearly unchanged. Meanwhile, the higher frequency edge for efficiency over 70% is extended from 2.7 to 3 GHz with the same lower frequency edge. The electrical lengths of TL1 and TL4 are 22.5° @ 3 GHz, which is 2.25° @ 0.3 GHz. At low frequencies, the electrical lengths of TL1 and TL4 are very short, leading to weaker coupling between them.

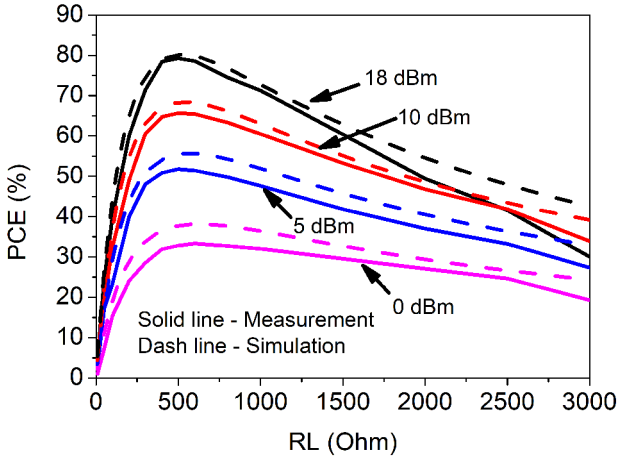

Figure 8. Simulated and measured PCE changing with the load resistances under different input power levels.

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Table 1. Comparison between the proposed rectifier and the references

Ref.	BW (GHz)	Relative BW	Efficiency over BW	Maximum efficiency	Size (mm^2)
[5]	2.08–2.58	21.5%	>70% @17.2 dBm	80.8% @17.2 dBm	126 × 68
[6]	2–3.05	41.5%	>70% @10 dBm	75.8% @14 dBm	36 × 35
[7]	0.57–0.9	44.9%	>70% @12.8 dBm	75% @15 dBm	85 × 61.5
[8]	0.47–0.86	58.6%	>60% @10 dBm	N.A.	178 × 6
[10]	0.1–2.5	184.6%	45% @10 dBm	74.8% @10 dBm	22.5 × 31
[12]	0.97–2.55	90%	>50% @10 dBm	65% @10 dBm	24 × 36
[13]	2.1–3.3	22.2%	>70% @14 dBm	76.3% @14 dBm	31 × 18
[14]	1.75–3.55	67.9%	>70% @10 dBm	76% @10 dBm	25 × 35
[15]	1.8–2.72	40.7%	>70% @19.5 dBm	80.3% @22 dBm	60 × 25
[17]	1–2.7	91.9%	>70% @15 dBm	78.2% @18dBm	38 × 15
[19]	0.06–1.82	187.2%	>70% @23 dBm	77.3% @23 dBm	20 × 7.4
This work	0.3–2.9	162.5%	>60% @18 dBm	79.8% @19 dBm	19 × 18

BW: bandwidth.

However, at high frequencies, their electrical lengths are longer, resulting in stronger coupling. Therefore, the coupling between TL1 and TL4 has a smaller impact on the rectifier at low frequencies.

In order to further investigate the effect of electrical lengths θ_1 and θ_2 on the input matching, the return loss performance is simulated by changing θ_1 and θ_2 in Fig. 4. As shown, with the increment of θ_1 and θ_2, the higher operating frequency edge moves towards the lower frequency. Compared with θ_2, although θ_1 only changes slightly for low frequencies, the lower operating frequency changes more noticeably. Here, the coupling plays an important role.

Implementation and measurement results

According to the above analysis, the initial dimensions of the rectifier can be obtained. Then, all the dimensions for the rectifier are optimized in ADS. The ultra-wideband rectifier, using Infineon BAT15-04 W Schottky diode, is fabricated on a 0.8 mm thick F4B substrate with a relative permittivity of 2.6 and a loss tangent of 0.002. Figure 5 depicts the layout and photograph of the fabricated rectifier with dimensions of 19 mm × 18 mm. The DC-blocking capacitor C_1 is 47 pF, the by-pass capacitor C_L is 180 pF, and the load R_L is 500 Ω.

The Agilent N5230A network analyzer with a maximum power of 14 dBm was used for $|S_{11}|$ measurement. The simulated and measured $|S_{11}|$ under power levels of 0, 5, 10, and 14 dBm are plotted in Fig. 6(a). The simulated $|S_{11}|$ is better than −10 dB at 14 dBm from 0.51 to 2.88 GHz, while the measured one is from 0.54 to 3 GHz. The measured results agree well with the simulated ones, except for a slight frequency shift, which may be attributed to fabrication and tolerance errors. Figure 6(b) depicts the simulated and measured PCEs changing with the frequency from 0.1 to 3.2 GHz when the input power is 0, 5, 10, and 18 dBm, respectively. These results confirm a good correlation between simulation and measurement. At an input power of 18 dBm, the simulated PCE is over 60% from 0.1 to 2.92 GHz, while the measured one is from 0.3 to 2.9 GHz. When the input power is reduced to 10 dBm, the measured PCE is still over 50% from 0.3 to 2.9 GHz.

Figure 7 shows simulated and measured PCEs and output DC voltage versus the input power at four typical frequencies, 0.3, 0.9, 1.6, and 3 GHz, respectively. The simulation and measurement agree well with each other, except for the best PCE point, which shows a notable discrepancy. This difference could be attributed to the breakdown voltage of the diode model being larger than the actual one. Also, the marginal difference observed between the measured and simulated results may be ascribed to the package parasitic effects, particularly notable at higher frequencies. In Fig. 7, at the four frequencies, the measured PCE reaches its maximum value of 65.8%, 79.8%, 75.2%, and 56.2%, respectively. At 0.9 GHz, the measured PCE is over 50% when the input power ranges from 5 to 22 dBm, with a dynamic range of 18 dB. Figure 8 shows the simulated and measured PCE changing with the load at 0.9 GHz when the input power is 0, 5, 10 and 18 dBm. As shown, the optimal load resistance of the rectifier is about 500 Ω. The measured PCE is slightly lower than the simulated PCE. When the load is larger than 1500 Ω, and the input power is 18 dBm, the measured PCE is much lower than the simulated one. In the simulation, the diode operates before breakdown, whereas in the measurement, the diode has undergone breakdown, leading to a significant drop in efficiency. It should be noted that the breakdown voltage specified in the model is higher than the diode's actual breakdown voltage.

The performance comparison of the proposed ultra-wideband rectifier and the recently published works in the literature is listed in Table 1. As shown, the proposed rectifier has a broader bandwidth than the majority of rectifiers, surpassing all except for those in papers [10] and [19]. Notably, the efficiency over bandwidth in paper [10] is 45%, while our design achieves 60%. Additionally, the rectifier in paper [19] operates at a much lower frequency of 0.06 GHz compared to our rectifier's 0.3 GHz. Moreover, our design has a smaller size compared to the other works. In summary, our design showcases the merits of high efficiency, broad bandwidth, and compact size.

Conclusion

This paper presents a compact and ultra-wideband microwave rectifier using an asymmetric coupled-line as the input impedance matching network. The rectifier, with dimensions of 19 mm × 18 mm, has a measured PCE of over 60% from 0.3 to 2.9 GHz (162.5% relative bandwidth) at an input power of 18 dBm. The high performance is attributed to the asymmetric coupled-line impedance transformer. The proposed rectifier can be applied in WPT applications where compact size and wide bandwidth are required.

Author contributions. Fei Cheng and Li Wu derived the theory and Chun-Hong Du performed the simulations. All authors contributed equally to analyzing data and reaching conclusions, and in writing the paper.

https://doi.org/10.1017/S1759078724000813 Published online by Cambridge University Press

Funding statement. This work was supported by the foundation of National Key Laboratory (Grant No. 2023-JCJQ-LB-051-06).

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