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A Q-/V-band 37.6-dBm $IP_{0.1\ dB}$ and low loss SPDT switch using three-series PIN diodes connection

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Research Paper

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Abstract

This manuscript presents a novel three-series-only topology P-insulator-N (PIN) diode single-pole-double-through (SPDT) switch designed to address the challenges of high power handling and low insertion loss in Q-band and V-band communication systems. The manuscript provides a detailed theoretical analysis of series-connected PIN diodes, offering insights into their behavior under both small- and large-signal conditions. Based on GaAs PIN diode technology, the switch operates across a frequency range of 37.7 to 61 GHz, achieving a low insertion loss of 0.707 dB and providing an isolation of 24.6 dB. The proposed SPDT switch demonstrates a high $IP_{0.1\ dB}$ of 37.6 dBm at 38 GHz. With a compact chip size of $0.905 \times 0.885 mm^2$, including all pads, this work offers excellent power handling capability, making it highly suitable for advanced communication systems in Q-band and V-band applications.

Introduction

Single-pole-double-through (SPDT) switches play an essential role in wireless front-end systems, which control the direction of RF signal between the transmitting and receiving (Tx/Rx) modes [1–3]. In general, SPDT switches require a low insertion loss (IL) to minimize system noise in Rx mode and sufficient power handling capability to fully transfer RF power from the power amplifier (PA) to the antenna in Tx mode.

However, in most SPDT switch designs, IL and power handling are typically a trade-off. Therefore, achieving both low IL and high power handling SPDT switches is a key challenge.

Additionally, bandwidth, isolation, and switching speed are also critical characteristics of SPDT switches.

Switches are composed of devices, such as FETs and diodes, that can switch between on and off states. The impedance between the drain and the source of an FET can be controlled by altering its gate voltage. In millimeter-wave frequencies, FETs are often used to design SPDT switches, including those based on CMOS [4], pHEMT [5, 6], and mHEMT [7] technologies, to achieve low-loss and wideband performances. However, most FET switches have an input 1-dB compression point ($IP_{1\ dB}$) of less than 25 dBm, making them unsuitable for handling the high output power from a PA. To enhance $IP_{1\ dB}$, [8, 9] using the SOI process with a stacked-FET structure to improve the IP_{1dB}, which can achieve 29 dBm at 30 GHz.

Owing to CMOS process limitations, stack FET can improve power handling but get higher IL.

Through the use of GaN process, which has favorable high-power characteristics, a high-$IP_{1\ dB}$ of 49.5 dBm at 27 GHz [10] can be achieved. Although [8, 10] have good $IP_{1\ dB}$, their IL are high.

As mentioned earlier, the SPDT switch needs low IL, high isolation, high switching speed, and high $IP_{1\ dB}$ (high power handling) at the same time. FET devices and GaN process can only satisfy part of these characteristics. To realize this performance, using P-insulator-N (PIN) diodes as switch devices is the best choice. Due to their low series resistance, high breakdown voltage, and fast switching speed, PIN diodes are extensively utilized in SPDT switch design.

For realizing SPDT switches using PIN diodes, several topologies can be considered, including shunt-series, series-shunt, shunt-only, series-only, and anti-series configurations. [11] used two shunt PIN diodes to realize low loss at E-band and W-band. [12] used traveling waves with four shunt PIN diodes for wide-band design. A novel series-shunt topology with a resistive bias network at 60 GHz is shown in [13] to reduce chip area. But its $IP_{1\ dB}$ only has 22 dBm and 2 dB IL. [14] also used series-shunt topology for wide-band and compact-size SPDT switch design. It has 25.5 dBm $IP_{1\ dB}$ and 70 GHz bandwidth. [15] used two series diodes for high $IP_{0.1\ dB}$ at Ka-band.

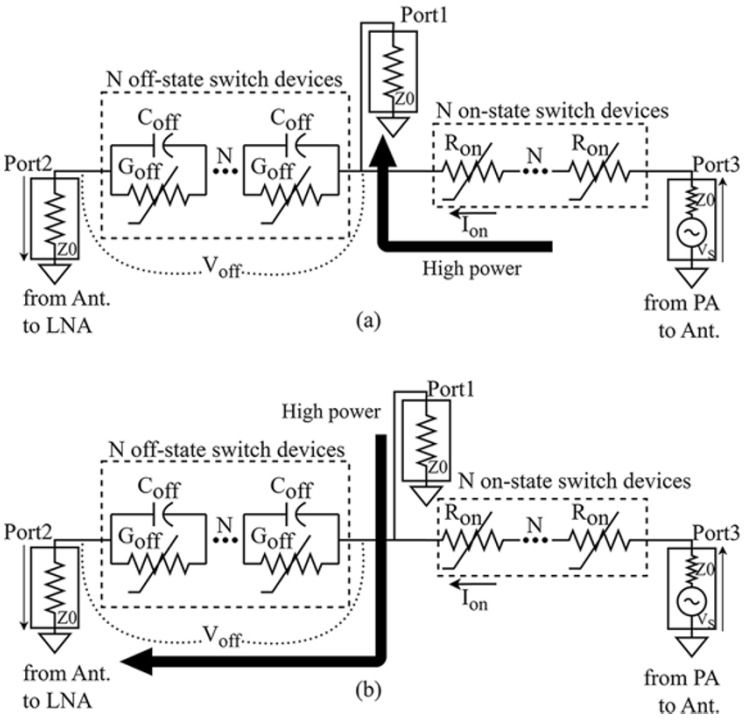

Figure 1. Block diagrams of an SPDT switch when measurements of (a) insertion loss and (b) isolation were performed.

However, the power handling of these designs has not yet been optimized in theory.

In this work, the primary design goal was to achieve extremely low IL and high power handling capability, which are critical for high-performance front-end systems in millimeter-wave applications. As such, isolation and bandwidth were not specifically optimized. Nonetheless, compared to other published works using GaAs PIN diode processes, the isolation and bandwidth of this work remain competitive, particularly given the higher operating frequency range of the proposed design.

This manuscript presents a novel three-series-only topology PIN diode SPDT switch that specifically addresses the challenges of high power handling and low IL in Q-band and V-band. The proposed SPDT switch demonstrates an $IP_{0.1\,dB}$ of 37.6 dBm at 38 GHz, which is the best among PIN diodes-based SPDT switches in the literature [11]-[15], [17]. Additionally, it achieves an IL lower than 1.5 dB across the 37.7-61 GHz range, with a minimum IL of 0.707 dB at 53 GHz. More importantly, this work is the first to provide a comprehensive analysis of the behavior of series-connected PIN diodes, enabling the design to achieve high $IP_{0.1\,dB}$ and low loss across both the Q-band and V-band. This theoretical foundation not only supports superior performance but also highlights the suitability of PIN diodes for high-power, low-loss applications. The impact of the number of series-connected PIN diodes on the power handling of the SPDT switch is also explored in the manuscript.

Circuit design

Figure 1 shows a general series topology SPDT switch equivalent block diagram. The series switch is composed of series-connected switching devices with N devices. In the on-state, the switching devices can be modeled as resistors (R_{on}), while in the off-state, they can be modeled as capacitors (C_{off}). Under large-signal operation conditions, the off-state switching devices have a leakage current. Therefore, non-zero conductance (G_{off}) is added to model the effect of the leakage current in the large signal. $R_{on,eff}$ denotes the total on-state resistance of the N-series connected switching devices, while $C_{off,eff}$ and $G_{off,eff}$ represent the equivalent off-state capacitance and conductance in parallel, respectively. Under small-signal conditions, there is no leakage current; thus, G_{off} is zero. This switch is symmetric in design; in this case, the off-state device connects to LNA, and the on-state device connects to PA.

In this work, the simplified model [16] was adopted for analysis. According to [16], the simplified model can provide accurate simulation results up to at least 50 GHz. The simplified model of the PIN diode is shown in Fig. 2. The on-state model is represented as an inductor series with a resistor (R_{on}), and the off-state model is represented as an inductor series with a resistor (G_{off}) and capacitor (C_{off}). The parameters of the simplified model were extracted from the complete model provided by the foundry. Because the size of the PIN diode is small, the parasitic inductor effect is small enough to ignore. In other words, this simplified model can be further reduced to only two parameters (R_{on} and C_{off}).

IL in Fig. 1(a) is defined with respect to the signal from the PA to the antenna and can be evaluated as

$$\begin{aligned} \mathrm{IL} &= \frac{2/\left(\frac{1}{\frac{1}{j\omega C_{off,eff}+G_{off,eff}}+Z_0}+\frac{1}{Z_0}\right)}{\left(\frac{1}{\frac{1}{\frac{1}{j\omega C_{off,eff}+G_{off,eff}}+Z_0}+\frac{1}{Z_0}}+Z_0+R_{on,eff}\right)} \\ &= \frac{2Z_0(j\omega C_{off,eff}Z_0+G_{off,eff}Z_0+1)}{K+G_{off,eff}Z_0(3Z_0+2R_{on,eff})+2Z_0+R_{on,eff}}, \end{aligned} \tag{1}$$

where $K = j\omega C_{off,eff}Z_0(3Z_0+2R_{on,eff})$, $R_{on,eff} = R_{on_1}+R_{on_2}+\cdots+R_{on_N}$, $C_{off,eff} = C_{off_1}\|C_{off_2}\|\cdots\|C_{off_N}$, and $G_{off,eff} = G_{off_1}\|G_{off_2}\|\cdots\|G_{off_N}$ and Z_0 is the characteristic impedance of the system by using simplified model. Isolation (ISO) in Fig. 1(b) is defined with respect to the leakage signal from the antenna to the

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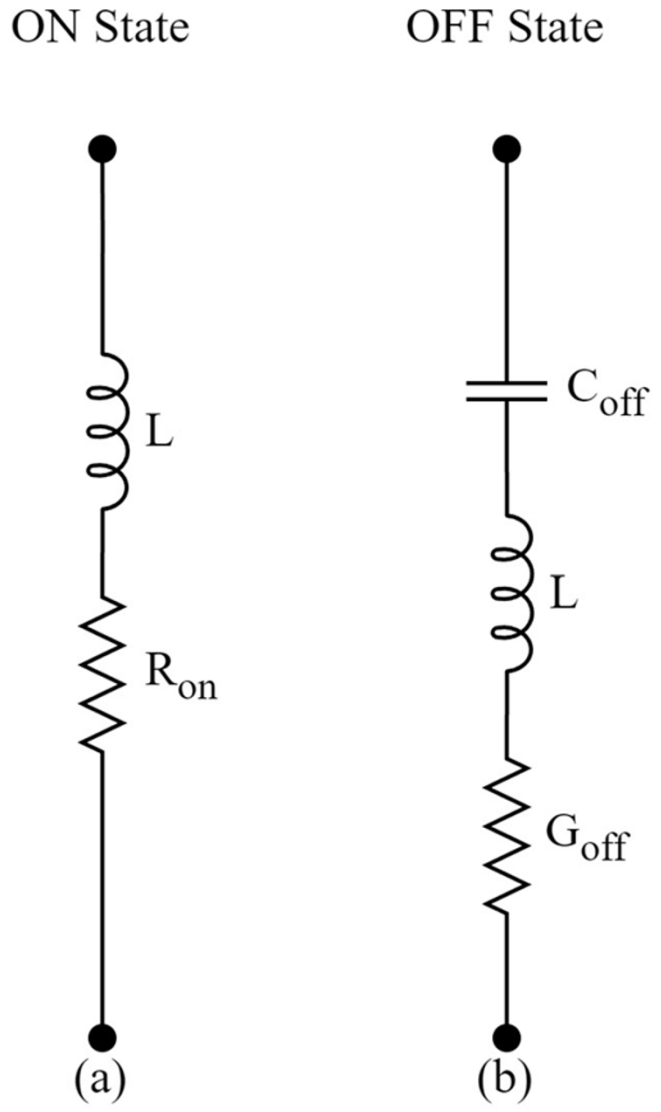

Figure 2. Simplified models for (a) on- and (b) off-state PIN diode [16].

low-noise amplifier and can also be expressed as

$$\begin{aligned}\text{ISO} &= \frac{2}{\left(\frac{1}{R_{\text{on,eff}}+Z_0}+\frac{1}{Z_0}\right)\left(\frac{1}{j\omega C_{\text{off,eff}}+G_{\text{off,eff}}}+\frac{1}{\frac{1}{Z_0+R_{\text{on,eff}}}+\frac{1}{Z_0}}+Z_0\right)} \\ &= \frac{2j\omega C_{\text{off,eff}}Z_0(Z_0+R_{\text{on,eff}})+2G_{\text{off,eff}}Z_0(Z_0+R_{\text{on,eff}})}{K+G_{\text{off,eff}}Z_0(3Z_0+2R_{\text{on,eff}})+2Z_0+R_{\text{on,eff}}}.\end{aligned} \quad (2)$$

where $K = j\omega C_{\text{off,eff}}Z_0(3Z_0 + 2R_{\text{on,eff}})$, $R_{\text{on,eff}} = R_{\text{on}_1} + R_{\text{on}_2} + \cdots + R_{\text{on}_N}$, $C_{\text{off,eff}} = C_{\text{off}_1}\|C_{\text{off}_2}\|\cdots\|C_{\text{off}_N}$, and $G_{\text{off,eff}} = G_{\text{off}_1}\|G_{\text{off}_2}\|\cdots\|G_{\text{off}_N}$ and Z_0 is the characteristic impedance of the system. It is noted that G_{off} is zero under small-signal conditions because there is no leakage current. When R_{on}, C_{off} and G_{off} in (1) and (2) are approximately 0, IL is 0 dB and ISO is -∞ dB. This consists of the performance of an ideal switch. Therefore, under small-signal conditions, minimizing the values of R_{on} and C_{off} is crucial for achieving an RF switch design with low IL and high ISO.

The verification of formulas (1) and (2) is shown in Fig. 3, which compares the SPDT switch's IL and isolation obtained from the simulation and analysis. From Fig. 3, it can be observed that the two lines of IL and isolation exhibit close agreement. The gap is about 0.11-0.14 dB. Therefore, the analysis results of formulas (1) and (2) are similar to the simulation result of the complete model.

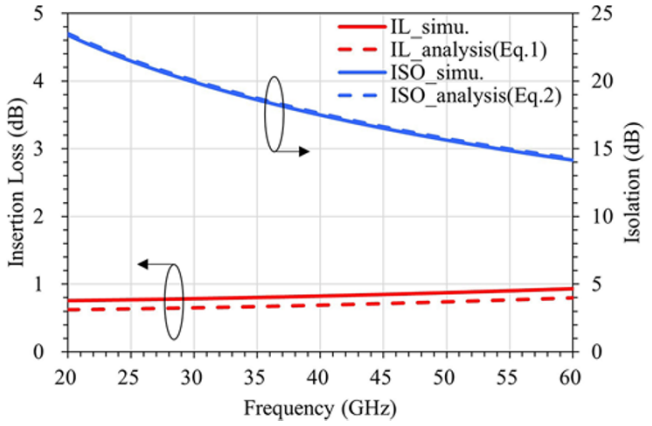

Figure 3. Comparison of insertion loss and isolation between the simplified and complete models of the SPDT switch.

In general, R_{on} is inversely proportional to device size; whereas C_{off} and G_{off} are proportional to device size. Under large-signal conditions, G_{off} denotes the leakage current, which is usually small compared with the admittance of $j\omega C_{\text{off}}$ at high frequency. It is important to choose the process and the device size having small $R_{\text{on}}C_{\text{off}}$.

Due to its inherently small $R_{\text{on}}C_{\text{off}}$, the PIN diode was selected in this GaAs-based SPDT switch design. The process is a commercial GaAs process. In this process, there are three device options (pHEMT, Schottky diode, and PIN diode) for switch design. Table 1 presents the values of R_{on}, C_{off}, and $R_{\text{on}}C_{\text{off}}$ of the switch devices. The R_{on} and C_{off} values in Table 1 were extracted from the complete model provided by the foundry. Compared to pHEMT and Schottky diode, the PIN diode has a lower value of $R_{\text{on}}C_{\text{off}}$, indicating its potential for achieving low IL and high ISO under small-signal conditions.

Under large-signal conditions, it is necessary to discuss the effects of the high power on the parameters of the models (R_{on} and G_{off}). Fig. 4 (a) presents the dynamic current versus the voltage of the PIN diode; Fig. 4(b)(c) presents the current waveform of small and large signals in different states. In the on-state, increasing the input power leads to a larger voltage and current swing. If the current swing reaches the lower boundary of the linear operation region of the device (In this case, 0 A is the lower boundary), the dynamic current will be cut off. Therefore, a part of the lower half of the current waveform is cut off, and there is no significant influence on the upper half of the current waveform. The waveform distortion alters the ratio of average current to voltage, thereby affecting the impedance at the operating frequency. In the off-state, the leakage current appears when a large voltage or current swing is applied, and leads to the effect of G_{off}. As illustrated in Fig. 4(b), V_{off} determines the maximum voltage swing preventing leakage current. Therefore, V_{off} is an important biasing point for high-power operation.

In Figs. 4(a), (b), and (c), the linear region is determined by the voltage or current swing. It is necessary to evaluate the relationship between the input power and the voltage swing. In Fig.1(a) and (b), the input power to Port 1 or Port 3 can be expressed as $V_s^2/8Z_0$. This derivation assumes that the switch loss is negligible ($j\omega C_{\text{off}} \approx 0$).

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Table 1. Comparison of R_{on} and C_{off} values for GaAs HEMT, Schottky diode, and PIN diode.

pHEMT	$R_{on}(\Omega)$	$C_{off(fF)}$	$R_{on}C_{off}(\Omega\cdot fF)$	**PINdiode**	$R_{on}(\Omega)$	$C_{off(fF)}$	$R_{on}C_{off}(\Omega\cdot fF)$
2 × 20μm	21.675	52	1127.1	10μm × 10μm	2.185	17	37.145
2 × 50μm	9.792	43	421.056	20μm × 20μm	2.043	36	73.548
2 × 75μm	6.607	54	356.778	30μm × 30μm	1.845	71	130.995
2 × 100μm	2.332	120	399.84	40μm × 40μm	1.603	137	219.611
Schottkydiode	$R_{on}(\Omega)$	$C_{off(fF)}$	$R_{on}C_{off}(\Omega\cdot fF)$	50μm × 50μm	1.338	270	361.26
1 × 20μm	14.667	38	557	10μm × 10μm × 2	4.481	10.5	47.05
2 × 20μm	7.312	67	490	10μm × 10μm × 3	7.132	10	**71.32**
4 × 10μm	6	75	450	10μm × 10μm × 4	10.341	9.5	98.24
4 × 20μm	3.93	136	534	10μm × 10μm × 5	14.7	9	132.3

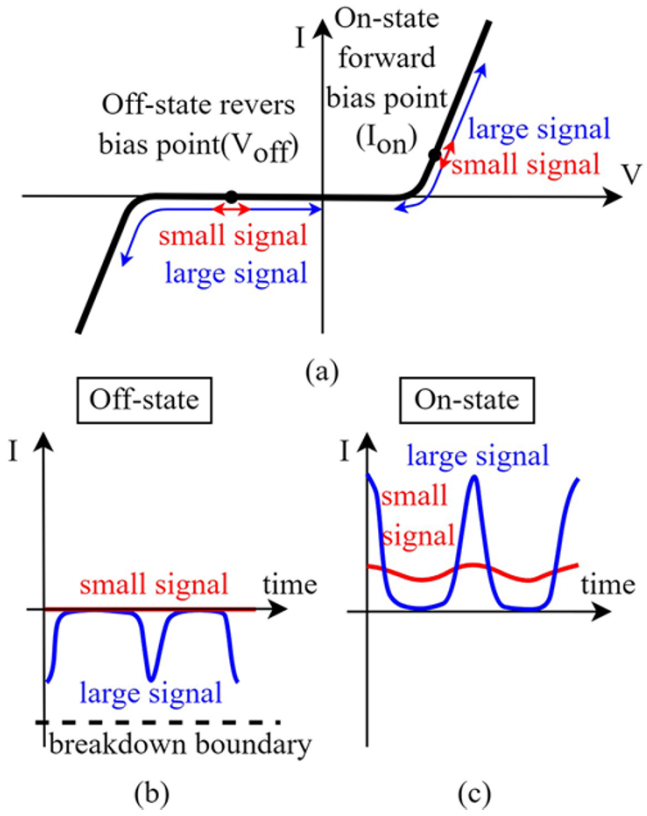

Figure 4. (a) Dynamic voltage-current waveforms of a PIN diode at high and low power levels (P_{in}). (b) Off-state and (c) On-state current waveform of small and large signals.

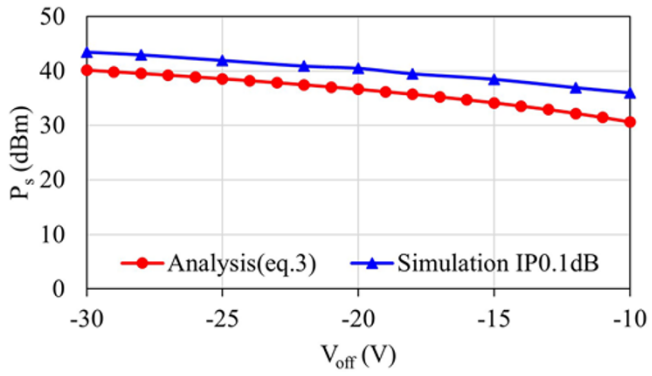

Figure 5. Comparison of V_{off} versus P_s from analysis and simulation.

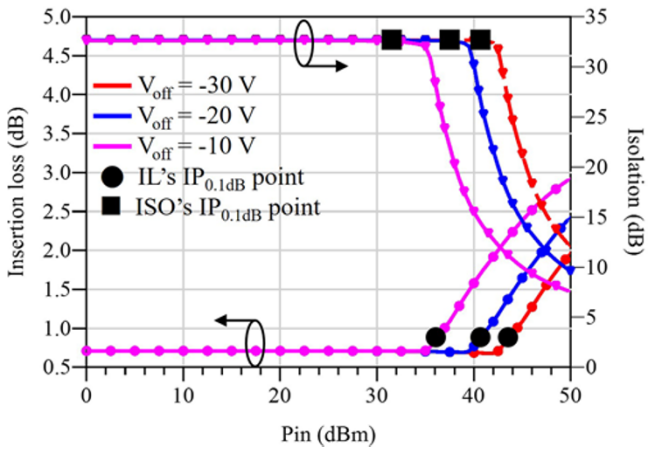

Figure 6. Simulation of the SPDT switch's power performance with different V_{off}.

The voltage of the off-state device (V_{off}) in both states [Fig. 1(a) and Fig. 1(b)] can be approximated as

$$V_{off} = \sqrt{P_s}(2Z_0)^{\frac{3}{2}}/(2Z_0 + R_{on,eff}). \quad (3)$$

where P_s means the power level that the switching devices can afford. In the case of a 50 Ω system impedance, the R_{on} and C_{off} values of the three series-connected 10×10μm PIN diodes from Table 1 were substituted into (3). This substitution yielded an approximate expression of $V_{off} \approx 9.34\sqrt{P_s}$ (V), where P_s is expressed in units of Watts (W). Therefore, when V_{off} is 30 V, the SPDT switch can afford at least 10 W (i.e., 40 dBm).

Figure 5 compares the calculated P_s values from formula (3) (red curve) with the simulated $IP_{0.1\,dB}$ values (blue curve). The close alignment between the two curves validates the analytical model's reliability in predicting SPDT switch behavior under varying V_{off} conditions. This comparison highlights the effectiveness of formula (3) as a rapid estimation tool for high-power switch design. The minor gap, caused by nonlinear coefficients excluded in the analytical model, remains within acceptable limits and does not compromise the accuracy of the analysis.

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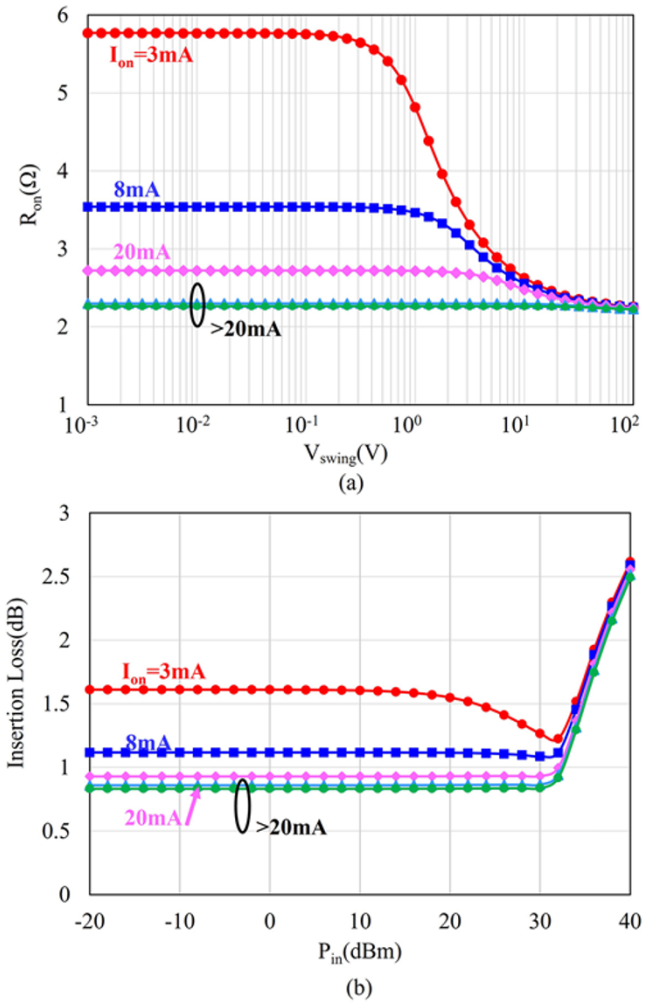

Figure 7. (a)R_{on} versus V_{swing} and (b) insertion loss at different I_{on}

Figure 6 shows the relationship between the power performance and V_{off}.

When $V_{off} = 30, V$, the SPDT switch operates in the linear region up to $P_{in} = 40, dBm$, and the $IP_{0.1\,dB}$ reaches approximately 43 dBm. This verifies that the power handling capability of the SPDT switch can be designed by selecting an appropriate V_{off} bias. The limit V_{off} is the breakdown voltage, which is determined by the process and must be greater than $2V_{bias,\,off}$ (60 V). One GaAs PIN diode has a breakdown voltage as high as 80 V, which is significantly greater than that of GaAs pHEMTs and Schottky diodes. Moreover, the breakdown voltage can be enhanced by series-connected topology. Table 1 shows the $R_{on}C_{off}$ values of $10\mu m \times 10\,\mu m$ diodes connected in series in varying numbers. The $R_{on}C_{off}$ of three PIN diodes connected in series is lower than a PIN diode with 20 μm × 20 μm. Therefore, to achieve a higher $IP_{1\,dB}$, three series-connected PIN diodes with a breakdown voltage up to 240 V are more suitable than two or one.

For the biasing selection of I_{on}, it determines R_{on} and influences the small signal IL. In Fig. 7(a), the simulation shows that R_{on} of the PIN diode decreases as the power level increases, which is consistent with the analysis in [17, 18]. According to (1), small R_{on} makes IL better; the change of R_{on} in high power level even helps to improve the IL in this series switch. In the small signal region (small V_{swing}) of the simulation results in Fig. 7(a), higher I_{on} leads to smaller R_{on}. However, the difference between R_{on} with $I_{on} > 20$ mA and with $I_{on} = 20$ mA is only 0.5 Ω, but the power consumption more than triples. Figure 7(b) presents the IL for various I_{on} for switch designs in which V_{off} is set to 10 V to prevent voltage swings over the breakdown voltage and ensure that $G_{off} = 0$. The losses are higher for I_{on} below 20 mA, and the losses at $I_{on} = 20$ mA and $I_{on} > 20$ mA only differ by 0.3 dB, but the power consumption is 3 times at the higher current. Hence, in this design, $I_{on} = 20$ mA was selected to achieve favorable IL with lower power consumption.

Chip implementation

The GaAs PIN diode process was used to produce the novel three-series SPDT switch topology. Figure 8(a) shows the complete SPDT switch circuit schematic.

The advantages of three PIN diodes connected in series are mentioned in Section II.

Figure 9 compares the performance of $IP_{0.1\,dB}$, ISO, and IL with different numbers of diodes.

The I_{on} conditions of all five simulations are identical, while the V_{off} conditions are directly proportional to the number of diodes.

Most commercial PAs in the mmWave range have output powers below 10 W, as shown in [19] and [20]. Additionally, [21] demonstrates that the output power of most academic PAs in the mmWave range is also below 10 W. Thus, the design target for $IP_{0.1\,dB}$ was set to 10 W.

Since IL significantly impacts the performance of the front-end system, minimizing IL is a critical design goal. Regarding ISO, it is intuitive that increasing the number of diodes enhances isolation. However, for the SPDT switches in practical system applications, an isolation of 25 dB is sufficient. Therefore, a 3-diode configuration is well-suited for this design.

Three 10 μm × 10 μm diodes are connected in series as switch devices at both the Tx and Rx paths; R_{on} and C_{off} are 7.13 Ω and 10 fF, respectively. Although using a series architecture increases the equivalent R_{on}, the breakdown voltage may increase, enhancing the power handling capability of the SPDT switch. Additionally, the series topology reduces the equivalent C_{off} of the series structure.

The breakdown voltage of a single PIN diode is 80 V. Therefore, the breakdown voltage of these three diodes connected in series can reach as high as 240 V. The $IP_{1\,dB}$ of this SPDT switch can support high input power due to the high breakdown voltage. In this design, the V_{off} is set to 30 V for the convenience of measurement.

When IL is very low, the reflection coefficient becomes a dominant factor affecting overall performance. Therefore, a matching network is needed in this design. Figure 8 (a) shows the SPDT switch's schematic. In order to minimize IL, the non-series matching network is used at port 2 and port 3. First, a high-impedance short stub is used to bring impedance close to 50 Ω. Second, a series capacitance is added to finely tune the impedance to 50 Ω. At port 1, the matching procedure is shown in Fig. 10. Because the R_{on} and C_{off} are connected in parallel, the impedance is at the lower right of the Smith chart center.

A series transmission line brings the impedance closer to 50 Ω, and an added capacitance helps distribute impedance across frequencies around the center, thereby increasing bandwidth.

The polarities of D1–D3 and D4–D6 are consistent. This design is practical because the switch only requires a positive bias voltage and does not require a negative one. In conclusion, the topology of three diodes connected in series in this SPDT switch provides very high $IP_{1\,dB}$ and low IL. This SPDT switch is also suitable for

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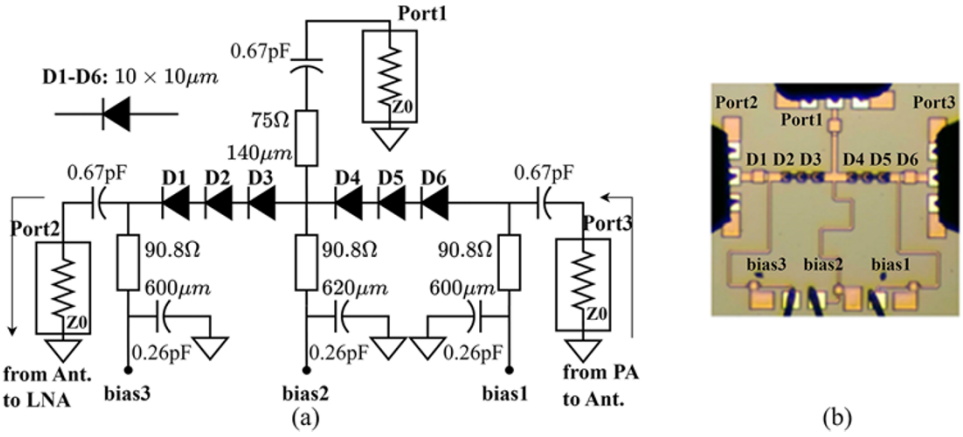

Figure 8. (a) Schematic and (b) chip photo (0.905×0.885 mm^2).

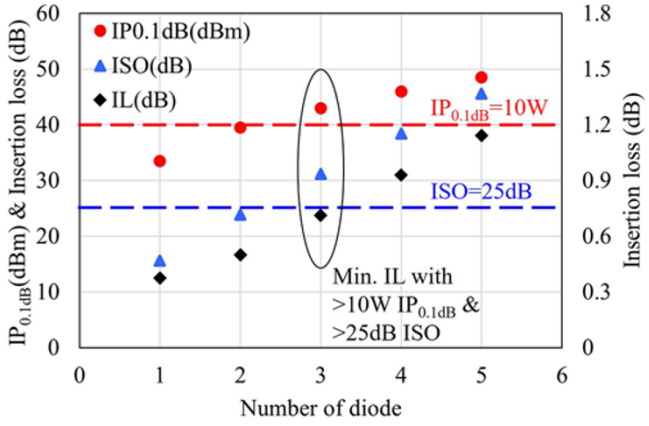

Figure 9. Simulation of the SPDT switch's $IP_{0.1\,dB}$, ISO and IL in different numbers of series diodes.

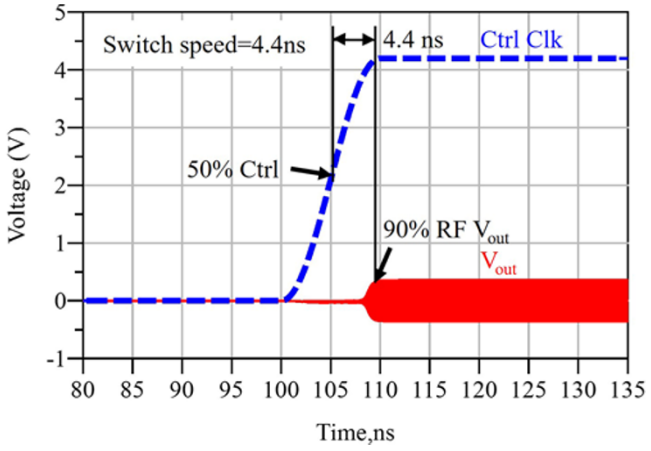

Figure 11. Simulation of the proposed SPDT switching speed.

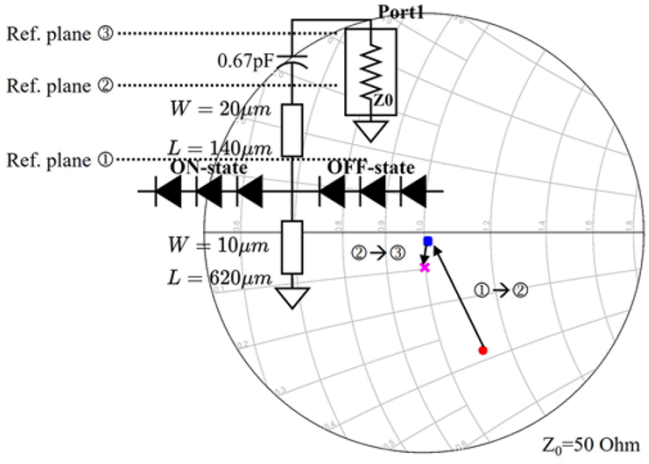

Figure 10. Matching procedure for Port 1.

the mm-wave system due to its wide bandwidth and positive bias control.

PIN diodes also exhibit high switching speed. The simulation of the switching speed is shown in Fig. 11. From Fig. 11, the switch-on time is approximately 4.4 ns, indicating a fast switching speed. For comparison, the SPDT switch designed using the GaAs pHEMT process has a switch-on time of about 6 to 10 ns. This further highlights the advantages of using PIN diodes for SPDT switch design.

Measurement results

A micrograph of the proposed SPDT switch is shown in Fig. 8(b). This SPDT switch was fabricated using a GaAs PIN commercial process provided by WIN Semiconductor, and the chip size, including the pads, was 0.905 × 0.885 mm^2. Circuit- and EM-level simulations were performed using Keysight ADS and ADS Momentum, respectively. The chip was measured using the on-wafer probing technique , and a standard SOLT calibration method was applied to de-embed the measurement reference plane to the probe tips.

Before calibration, the parasitic parameters of the probes, including C_{open}, L_{short}, and L_{load}, were input into the vector network analyzer to improve calibration accuracy. After calibration, the thru characteristics between any two ports were checked to verify the calibration quality before measuring the chip.

Figure 12 shows the large signal measurement setup. Owing to the high $IP_{1\,dB}$ performance of this SPTD switch, QuinStar's

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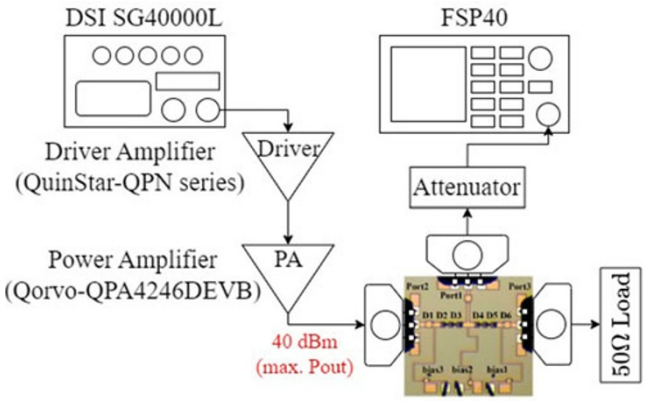

Figure 12. Measurement setup for large signal.

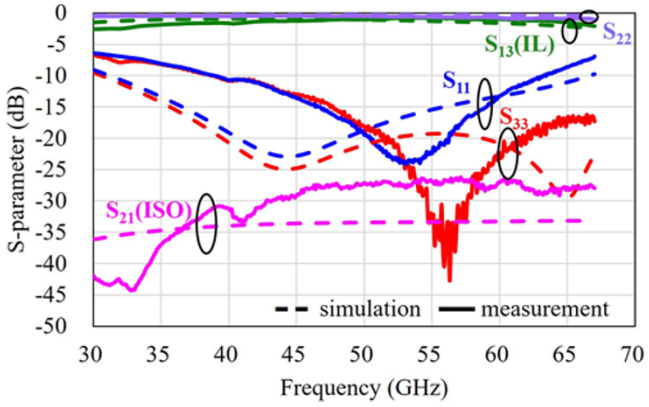

Figure 13. Measurement results for S-parameters.

driver amplifier and Qorvo's high-PA were used at the input port to extend the input power level and measured the SPDT switch's IP_{1dB}. QuinStar's driver amplifier can output 30 dBm from 36 to 39 GHz, while Qorvo's high PA can output 40 dBm from 37.5 to 42.5 GHz. After passing through the cable and probe following Qorvo's high PA, the input power to the SPDT switch chip was 37.6 dBm due to the loss of the cable and probe. Using the R&S signal analyzer FSP40 at the output port to measure the output level and add a 20 dB attenuator to protect the signal analyzer. The other port uses a probe with 50 Ω load to ensure the SPDT switch works normally.

Measurement condition, $I_{bias,\ on}$ and $V_{bias,\ off}$, were set to 20 mA and 30 V, respectively. Figure 13 and Fig. 14 show the small-signal performance measured using the Microwave Network Analyzer (Keysight N5247B). The operational frequency of the switch was 37.7–61 GHz, and its reflection coefficients were lower than -10 dB. The IL (-dB[S_{13}]) was lower than 1.5 dB for the entire frequency band, and the minimum value was 0.707 dB at 53 GHz. This represents a very low IL for mm-wave frequencies. The isolation (-dB[S_{21}]) was higher than 25 dB for the entire frequency band.

The achieved isolation of $>$ 25 dB across 37.7 – 61 GHz ensures sufficient suppression of undesired signals, meeting the requirements of high-frequency communication systems. Additionally, the wide bandwidth enhances the switch's adaptability for multi-band applications, making it highly suitable for Q-/V-band systems.

A driver amplifier and high PA are used for large signal measurements to extend the input power level of the SPDT switch up to

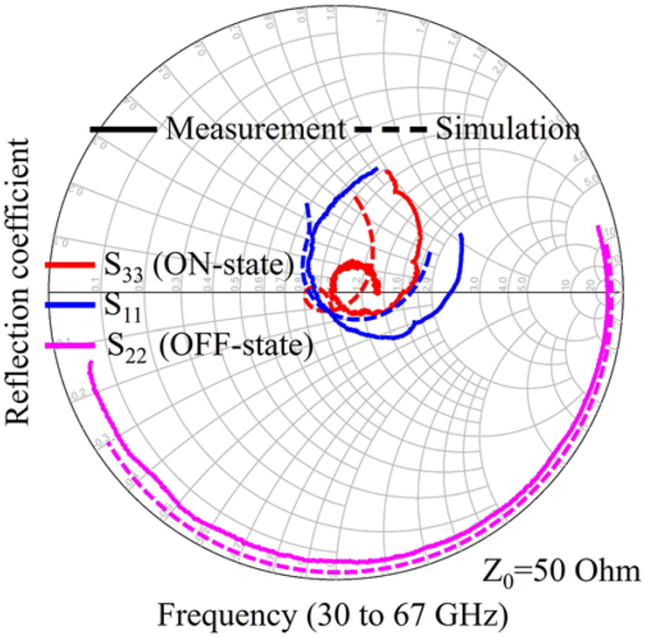

Figure 14. Measurement results for reflection coefficients.

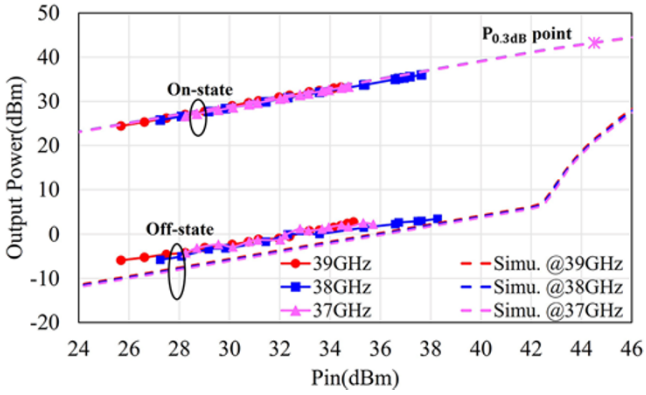

Figure 15. Measurement results for the SPDT switch's power performance.

37.6 dBm (including the loss from PA to the chip). The power measurement results at 37 to 39 GHz are shown in Fig. 15. The small signal loss of the switch at 38 GHz was 1.3 dB. With maximum input power (37.6 dBm), the IL at 38 GHz is compressed to 0.1 dB. In other words, $IP_{1\ dB}$ is much higher than 37.6 dBm. Therefore, this SPDT switch operated in a highly linear region during this high-power measurement. Furthermore, theoretically, increasing $V_{bias,off}$ results in higher $IP_{1\ dB}$.

Table 2 summarizes the performance of the proposed switch and other published works for comparison. This proposed SPDT switch has favorable performance regarding IL and $IP_{0.1\ dB}$ in millimeter-wave. The proposed FoM, shown in Table 2, is adapted from [24] and further modified to include the chip area in the denominator, providing a more rigorous and challenging evaluation of SPDT switch performance, particularly for compact designs. The FoM at present is higher than that of most of the other published works. Among SPDT switch designs utilizing PIN diodes, the FoM of this work is the highest. Compared to [10], this work has lower IL, chip size, and higher operating frequency.

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Table 2. Performance summary and comparison of SPDT switches.

Ref.	Process	Frequency (GHz)	Bandwidth (%)	Insertion loss (dB)	$IP_{0.1\ dB}$ (dBm)	$IP_{1\ dB}$ (dBm)	Isolation (dB)	Chip size (mm^2)	FoM
2021ISAP[11]	GaAs PIN Diode	55-105	62.5	Min. 2.8	-	-	10-30	-	-
2019MWCL[5]	GaAs 0.15-um pHEMT	36-38	5.4	3.2	*10	12 @37 GHz	> 28	1 × 1.1	-15.97
2017MWCL[6]	GaAs 0.1-um pHEMT	35-70	66.7	2.2-2.9	*16	20.2 @31 GHz	> 40	1.2 × 0.8	28.43
2013MWCL[22]	GaN PIN diode	20-27	29.8	3.1-3.4	*> 21	*> 21 @20 GHz	> 27	2.57 × 1.03	9.25
2020MWCL[7]	InGaAs mHEMT	42.5-76	56.5	1-1.7	> 22	> 22	29.7-32.8	1.5 × 1	41.3
2018APMC[14]	GaAs PIN diode	0.01-70	200	Min. 1.1	*20	25.5 @2 GHz	20	0.75 × 0.57	49.47
2019RFIC[13]	SiGe PIN Diode	38-67	55.2	Min. 2	*18	22 @60 GHz	> 23	0.066	50.07
2023IMS[23]	GaAs PIN Diode	25-30	18.2	< 1.2	> 35	> 35	> 20	1 × 1	48.42
2009IMS[15]	GaAs PIN Diode	30-40	28.6	< 0.8	> 37	> 37	30	1.2 × 2.2	57.04
2022MWCL[10]	GaN 150-nm HEMT	18-42	80	< 2	*46	49.5 @27 GHz	> 32.2	3.7 × 0.51	78.23
This work	**GaAs PIN diode**	**37.7-61**	**47.2**	**0.707-1.5**	**37.6**	**> 37.6 @38 GHz**	**> 24.6**	**0.905 × 0.885**	**75.3**

*estimated from figure.
**FoM [GHz·W/mm²]=$20 \cdot log((IP_{0.1\ dB}[Watt] \cdot BW[GHz] \cdot ISO[dB])/(Area[mm^2] \cdot IL[dB]))$.

Conclusion

This paper presents a novel three-series-only topology SPDT switch using the GaAs process. Additionally, it provides a comprehensive analysis of the behavior of series-connected PIN diodes operating at low and high power levels,demonstrating that PIN diodes are the most suitable for designing a low-loss SPDT switch capable of handling high input power across both the Q-band and V-band. The proposed SPDT switch has excellent performance with a minimum loss of 0.707 dB at 53 GHz, a high $IP_{0.1\ dB}$ of up to 37.6 dBm at 38 GHz, and a wide operating frequency from 37.7 GHz to 61 GHz. The results presented in this paper provide valuable insights regarding the design of SPDT switches for Q-band and V-band communication applications.

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Competing interests. The authors report no conflict of interest.

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